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HEWLETT-PACKARD COMPANY
Intellectual Property Administration
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EXAMINER

UMEZ ERONINI, LYNETTE T

ART UNIT PAPER NUMBER

1765

DATE MAILED: 07/13/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary

Application No.

09/932,055

Applicant(s)

DODD, SIMON

Examiner

Lynette T. Umez-Eronini

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-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 07 March 2005.
- 2a) ☐ This action is FINAL. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1-14 and 21-26 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 1-14 and 21-26 is/are rejected.
- 7) ☐ Claim(s) _____ is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☒ The drawing(s) filed on 16 August 2001 is/are: a) ☒ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some * c) ☐ None of:
- ☐ Certified copies of the priority documents have been received.
 - ☐ Certified copies of the priority documents have been received in Application No. _____.
 - ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).
- * See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- 1) ☒ Notice of References Cited (PTO-892)
- 2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
- 3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)
Paper No(s)/Mail Date _____
- 4) ☒ Interview Summary (PTO-413)
Paper No(s)/Mail Date: 3/10/2005
- 5) ☐ Notice of Informal Patent Application (PTO-152)
- 6) ☐ Other: _____

DETAILED ACTION

This communication is in response to Applicant's Remarks in Amendment filed 3/7/2005 and request for reconsideration of the 112(1) rejection of claim 11 in an Interview on 3/10/2005. Applicant's argument was persuasive in showing support (see Specification, Fig. 8 and paragraph [0021]) for "wherein the trench extends form a surface of the substrate on which the layer is provided only part of the way through the substrate" as recited in claim 11. Also previously allowed claims 1-10 and 21-26 have been withdrawn because the former prior art of record fail to teach the steps of etching a substrate surface as recited in the said claims, Hence a new Office action is presented.

Claim Rejections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

(e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

2. Claims 1-3, 5-7, 8, 10-14, and 21-26 are rejected under 35 U.S.C. 102(e) as being anticipated by Hostetler (US 6,675,476 B2).

As to claims 1-3, 5-7, 8, 10-14, and 21-26, Hostetler teaches, "The printhead structure **100** includes a silicon substrate **102** on which various patterned layers have

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been formed to fabricate the thin film structure, shown generally as **101** in FIG. **1B**. The thin film structure details will vary in dependence on the particular printhead design. FIGS. **1A-1B** illustrate in simplified form some of the patterned layers defining an exemplary thin film structure. These include a field oxide layer **104**, a polysilicon layer **106** (same as applicants' conductive material for a heat transducer), a passivation layer **108** including silicon carbide and silicon nitride layers, a tantalum layer **110** (same as applicant's metal layer) to define heating resistors for the printhead. Not shown, for example is an aluminum layer defining wiring traces" (column 4, lines 1-12).

"FIG. **1A** is a top plan view of the printhead structure **100** after the first step of the fabrication process, i.e. after the inkjet thin film structure has been formed on the silicon substrate. FIG. **1B** is a cross-sectional view of the printhead structure **100** after the TMAH etch process has been performed to create a break trench and after the barrier layer **112** is applied" (column 3, lines 61-67). The above reads on.

A method of etching a substrate surface, comprising the steps of:

masking a first portion of the substrate surface with passivation material having edges that define boundaries on the substrate surface such that within the boundaries a second surface portion is exposed for etching;

depositing a metal layer over the passivation material; and then

etching the second surface portion, **in claims 1, 21, and 22;**

wherein the masking step includes depositing a layer of silicon nitride on the substrate surface and the depositing on the silicon nitride a layer of silicon carbide, **in claim 2;**

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A method of etching a portion of a substrate surface, comprising the steps of:

masking the surface with passivation material having edges that define boundaries of the surface portion such that within the boundaries the surface portion is exposed for etching;

depositing a metal layer over the passivation material; and then

etching the surface portion and

fabricating on the substrate drop generator layers that provide for controlled expulsion of liquid from the substrate, and wherein the step of masking with the passivation material includes the simultaneous deposition of the passivation material at a location away from the exposed surface portion to enable use of some of the passivation material as one of the drop generator layers as well as the mask, **in claim 3;**

A method of etching a portion of a substrate surface, comprising the steps of:

fabricating on the substrate drop generator layers that provide for controlled expulsion of liquid from the substrate;

masking the surface with passivation material having edges that define boundaries of the surface portion such that within the boundaries the surface portion is exposed for etching;

depositing a metal layer over the passivation material; and then

etching the surface portion;

wherein the step of covering the passivation material with the metal layer includes the simultaneous deposition of the metal layer at a location away from the

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exposed surface portion to enable use of some of the metal layer as one of the drop generator layers, **in claim 5**;

A method of masking and etching a surface of a silicon substrate, comprising the steps of:

providing on the substrate surface an oxide in a pattern having edges that define boundaries of a surface portion such that within and adjacent to the boundaries the surface portion is exposed for etching;

covering the oxide layer near the edges with passivation material; and

etching the entire surface portion of the silicon substrate that is exposed for etching, **in claims 6-8 and 10**;

A method of fabricating multiple layer of a thermal inlet printhead that includes a substrate and a trench for moving ink across the substrate, as well as drop generator components for ejecting drops of ink from the substrate, comprising the steps of:

providing a layer on the substrate to serve as a drop generator component; and
then

etching the substrate to form the trench in the substrate, wherein the trench extends from a surface of the substrate on which the layer is provided only part of the way through the substrate, **in claims 11-14**; and

A method of etching substrate surface comprising:

depositing a passivation material on a first portion of the substrate surface and subsequently removing a portion of the deposited passivation material from a second

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portion of the substrate surface within the first portion, such that the second portion is free of passivation material;

depositing a metal layer over the passivation material and
etching the second portion, **in claims 23-26.**

Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

4. This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

5. Claims 4 and 9 are rejected under 35 U.S.C. 103(a) as being unpatentable over Hostetler (US 6,675,476 B2) as applied to claims 1 and 6 respective above, and further in view of Kawamura et al. (US 6,543,884 B1).

Hostetler differs in failing to the step of underlying the passivation material with a layer of phosphosilicate glass at locations near the boundaries, **in claim 4**; and temporarily covering the surface portion of the substrate with a layer of phosphosilicate glass that is removed before etching of the surface portion, **in claim 9**.

Kawamura teaches, " . . . ink ejection elements (same as applicant's drop generator), are formed on a top surface of a silicon substrate . . . An orifice layer is formed on the top surface of the thin film layers to define the nozzles and ink ejection chambers. A phosphosilicate glass (PSG) layer, providing an insulation layer beneath the resistive layers, is etched back from the ink feed holes and is protected by a passivation layer to prevent the ink from interacting with the PSG layer (Abstract). FIGS. **4**, **8**, and **10A – 10E**, and **11** show a plurality of thin films (column 4, lines 19-21), which comprises: FOX **92**, PSG **92**, TaAl **62**, Si₃N₄ **96**, SiC **98**, Ta **100**, and Au **114**.

Since Kawamura illustrates the step of underlying the passivation material with a layer of phosphosilicate glass (PSG) at locations near the boundaries and temporarily covering the surface portion of the substrate with a layer of phosphosilicate glass that is removed before etching of the surface portion and the use of PSG material in the manufacture of inkjet printhead is known, then it would have been obvious to one having ordinary skill in the art at the time of the claimed invention to modify Hostetler's technique of fabricating an inkjet printhead for the purpose of effecting the manufacture of a inkjet printhead.

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Any inquiry concerning this communication or earlier communications from the examiner should be directed to Lynette T. Umez-Eronini whose telephone number is 571-272-1470. The examiner is normally unavailable on the First Friday.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Nadine Norton can be reached on 571-272-1465. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

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July 7, 2005

NADINE G. NORTON
SUPERVISORY PATENT EXAMINER

